IN THE SPECIFICATION

Please replace the paragraphs on page 14, lines 10 through page 15, line 13 as shown below.

Further, processor 401 includes a watchpoint controller 403 that provides control information to a pipeline control unit 409 in order to stall and start an execution pipeline of processor 401. The watchpoint controller 403 may also keep track of watchpoint channel information in processor 401, and provide such information to circuit 402. Processor 401 also includes a branch unit 404 that handles branch-related instructions in processor 401, resolves/predicts branch addresses, and other branch-related functions. Branch unit 404 provides signals program counter information 414, CPU mode information ~~415~~ 421, and branch information ~~416~~ 422. Branch unit 404 also provides process identifier or ASID information 416. Processor 401 also includes a load-store unit 405 which is responsible for performing execution functions. Load-store unit 405 includes operand address (OA) watchpoints 406, which produce operand address information 415.

ASID information 416 and operand address (OA) information 415 are fed through multiplexer 417 and transmitted to debug circuit 402 via data line ~~417~~ 423. In one aspect of the invention, it is understood that when new ASID information 416 is available, no operand address information 415 will be available concurrently. Thus, the number of communication lines in communication link 420 are reduced because both ASID information 416 and OA information 415 are transmitted alternately over the same communication lines.

also includes a branch unit 404 that handles branch-related instructions in processor 401, resolves/predicts branch addresses, and other branch-related functions. Branch unit 404 provides signals program counter information 414, CPU mode information 415, and branch information 416. Branch unit 404 also provides process identifier or ASID information 416. Processor 401 also includes a load-store unit 405 which is responsible for performing execution functions. Load-store unit 405 includes operand address (OA) watchpoints 406, which produce operand address information 415.

ASID information 416 and operand address (OA) information 415 are fed through multiplexer 417 and transmitted to debug circuit 402 via dataline 417. In one aspect of the invention, it is understood that when new ASID information 416 is available, no operand address information 415 will be available concurrently. Thus, the number of communication lines in communication link 420 are reduced because both ASID information 416 and OA information 415 are transmitted alternately over the same communication lines.

Debug circuit 402 may include a trace buffer 418 to receive trace information produced by processor 401. Trace buffer may be, for example, a storage unit configured to receive and store information from processor 401. Trace buffer 408 may include control circuitry which detects whether trace buffer 418 can accept additional trace information from processor 401. If not, trace buffer may provide a stall indication 412 to watchpoint controller 403 which may, in turn, cause pipeline control 409 to stall the execution pipeline. When trace buffer 418 can accept additional trace information, trace buffer 418 may assert a different signal on stall 412 to indicate that buffer 418 can accept additional information. In another aspect, trace buffer operates in a mode whereby additional trace information is discarded if buffer 418 cannot accommodate additional trace information. Alternatively, buffer 418 can discard the oldest trace information first. Debug circuit 402 may also format trace messages into messages, which can be stored on chip (such as in the trace buffer 418) or spilled to memory or to an external communication port.

Debug circuit 402 may also include a state processor 419 which accepts state information from processor 401 such as watchpoint information from watchpoint controller 403, or operand address watchpoints from load store unit 405. State processor 419 may use the received state information as preconditions for watchpoints located in debug circuit 402. In a similar manner, state processor 419 may provide state values 413 to processor 401.

Table 1 below shows yet another embodiment of link signals according to one aspect of the invention shown with respect to Figure 5: